

# **METHOD FOR AN IMAGE REDUCING PROCESSING CIRCUIT**

## **FIELD OF THE INVENTION**

The present invention relates to a method for an image reducing  
5 processing circuit, and more particularly to the method for the  
image reducing processing circuit including a memory architecture  
of two First-In-First-Out (FIFO) units.

## **BACKGROUND OF THE INVENTION**

Recently, a hand-held image display system and a portable  
10 multimedia image display system mostly have smaller and lower  
resolution display element because of minimization and  
convenience. According to a signal resource such as signal of a  
television and a display card, the resolution of the signal resource  
has been defined in the past and is larger than the necessary  
15 resolution of the above-mentioned product (i.e., the above-  
mentioned image display system), and therefore it is more  
important to have a image processing circuit with the selective  
reduction of image and low power consumption.

A conventional method for image reducing processing circuit  
20 utilizes the architecture of a line buffer in order to get more  
completely image data in the subsequent process. An inputted  
image data is temporarily stored in a memory line by line and then  
is processed. Because the architecture of the line buffer is utilized,  
a memory implements the reading and writing and can processes

input image data and output image data with different frequency at the same time so as to increase the complexity of circuit. Furthermore, the memory stores the data of whole line, and therefore the requirement for the capacity of the memory is increased as well.

Referring to Figs. 1 and 2, the architecture of the image reducing processing circuit includes a pre-position data processing unit 10, a line buffer units 11, a vertical direction image processing unit 12, a horizontal direction image processing unit 13 and a post-position data processing unit 14. The image data (i.e., original images 1a) are firstly processed by the pre-position data processing unit 10, and then the original image 1a with the same first access frequency 1c is delivered to the line buffer units 11. According to the input sequence of the image data, the image data is stored to N sets of the line buffer 120, the vertical direction image processing unit 12, and the horizontal direction image processing unit 13 one by one. With the second frequency 1d, the image data is processed in parallel way by the line buffer unit 11 and finally delivered to the post-position processing unit 14 so as to output a reduced image 1b.

In conclusion, the size of the reduced image 1b is smaller than that of the input original image 1a in the above-mentioned architecture of the image reducing processing circuit. Because of using the architecture of the line buffer unit 11, the memory depth of the line buffer unit 11 will be designed and the same as that of the original image 1a. If the size of the input original image 1a is

much bigger than that of the output reduced image 1b, the capacity of the memory will be increased. The first frequency 1c and the second frequency 1d are used in the input and output of the line buffer unit 11 at the same time and are access frequency both, and  
5 therefore the circuit complexity of the memory during the memory implement the readout and writing of the image data at the same time.

Accordingly, there exists a need for the method for the image reducing processing circuit to solve the above-mentioned problems  
10 and disadvantages.

### **SUMMARY OF THE INVENTION**

The present invention to provide a method for an image reducing processing circuit including the memory architecture of two First-In-First-Out (FIFO) units for simplifying the using of access  
15 frequency and memory depth.

The method for the image reducing processing circuit according to the present invention includes the memory architecture of two First-In-First-Out (FIFO) units, and the method firstly processes the horizontal direction image data and then processes the vertical  
20 direction image data, such that the memory depth of the first step First-In-First-Out (FIFO) unit is designed and is only substantially equal to that of the reduced image. The memory depth of the first step First-In-First-Out (FIFO) unit is less than that of the line buffers. By using the memory architecture of two First-In-First-Out

(FIFO) units, the access frequency of the input processing unit, the horizontal direction image processing unit, the first step First-In-First-Out (FIFO) unit and the vertical direction image processing unit are simplified to the first access frequency only. The memory architecture of the second step First-In-First-Out (FIFO) unit is simplified to an one-input-one output-memory architecture, which only implements a transferring of the first and second access frequency, so the memory depth of the second step First-In-First-Out (FIFO) unit is much less than that the original image and the reduced image.

The foregoing, as well as additional objects, features and advantages of the invention will be more readily apparent from the following detailed description, which proceeds with reference to the accompanying drawings.

## **BRIEF DESCRIPTION OF THE DRAWINGS**

Fig. 1 is a block diagram of the architecture of an image reducing processing circuit with line buffers in the prior art.

Fig. 2 is a block diagram of the architecture of line buffers in the prior art.

Fig. 3 is a block diagram of the architecture of an image reducing processing circuit with two First-In-First-Out (FIFO) units according to the present invention.

Fig.4 is a block diagram of the architecture of an input processing unit and the horizontal direction image processing unit according to

the present invention.

Fig. 5 is a block diagram of the architecture of a first step First-In-First-Out (FIFO) unit according to the present invention.

Fig. 6 is a block diagram of the architecture of a vertical direction  
5 image processing unit according to the present invention.

Fig. 7 is a block diagram of the architecture of a second step First-In-First-Out (FIFO) unit and an output processing unit according to the present invention.

#### **DETAILED DESCRIPTION OF THE PREFERRED** 10 **EMBODIMENT**

Referring to Fig.3, which includes an input processing unit 20, a horizontal direction image processing unit 21, a first step First-In-First-Out (FIFO) unit 22, a vertical direction image processing unit 23, a second step First-In-First-Out (FIFO) unit 24 and an output  
15 processing unit 25. Image data (i.e., original images 1a) are firstly processed by the input processing unit 20 and then the original image 1a with the same first access frequency 1c delivered to the horizontal direction image processing unit 21. The horizontal direction image processing unit 21 receives the image data from the  
20 input processing unit 20, . The first step First-In-First-Out (FIFO) unit 22 receives the image data from the horizontal direction image processing unit 21 to read and write the image data with the same first access frequency 1c. The vertical direction image processing unit 23 receives the image data from the first step First-In-First-Out

(FIFO) unit 22, reads and writes completely the image data, quantifies the image data in the vertical direction, and then transfer the image data to row signals with a row column type. The second step First-In-First-Out (FIFO) unit 24 receives the image data from the vertical direction image processing unit 23 and transfers from the access frequency 1c to the access frequency 1d. The output processing unit receives the image data from the second step First-In-First-Out (FIFO) unit 25 and outputs the reduced image 1b on the access frequency 1d.

Referring to Fig. 4, the horizontal direction image processing unit 21 includes a horizontal direction data calculating element 210 and a horizontal direction data controlling element 211. The horizontal direction data calculating element 210 calculates in real time and processes the image data from the input processing unit 20 and the filtering parameter generated from the horizontal direction data controlling element 211 so as to generate new horizontal direction image data 2a, and the horizontal direction data controlling element 211 generates new image controlling signals XEN to control whether the image data are dumped or not.

Referring to Figs. 3, 4 and 5, the first step First-In-First-Out (FIFO) unit 22 includes N sets of First-In-First-Out (FIFO) sub unit (220, 221, 222, 223) receives and delivers the image data in sequence. As following up the image controlling signals XEN generated by the horizontal direction data controlling element 211, the image data from the horizontal direction image processing unit

21 are delivered step by step in sequence from the horizontal direction image processing unit 21 to the First-In-First-Out sub unit 220. Simultaneously, the First-In-First-Out sub unit 220 delivers the image data to next the First-In-First-Out sub unit 221, and  
5 another First-In-First-Out sub unit (220, 221, 222, 223) have similar logic way like the First-Out sub unit 220.

Referring to Figs. 3 and 6, the vertical direction image processing unit 23 includes a vertical direction data calculating element 230 and a vertical direction data controlling element 231. The vertical  
10 direction data calculating element 230 calculates in real time and processes the image data from the first step First-In-First-Out (FIFO) unit 22, the horizontal direction image data 2a generated from the horizontal direction image processing unit 21, and the filtering parameter generated from the vertical direction data controlling  
15 element 231 so as to generate new vertical direction image data 23a, and the vertical direction data controlling element 231 generates new image controlling signals YEN to control whether the image data are dumped or not.

Referring to Figs. 4, 6 and 7, the second step First-In-First-Out  
20 (FIFO) unit 24 includes a First-In-First-Out memory element 240 with N bit capacity implementing the readout and writing of the image data on two different frequency: the first access frequency 1c and a second access frequency 1d. As following up the image controlling signals YEN generated by the vertical direction data  
25 controlling element 231 and the image controlling signals XEN

generated by the horizontal direction data controlling element 211,  
and the vertical direction image data 23a from the vertical direction  
image processing unit 23 are delivered to the First-In-First-Out  
memory element 240 with N bit capacity on the access frequency  
5 1c. The output processing unit 25 includes an image processing  
element 250 and an output controlling element 251. The reading  
signal generated by the output controlling element 251 and  
delivered to the second step First-In-First-Out (FIFO) unit 24, and  
the image data are delivered to the image processing element 250  
10 on the second access frequency 1d so as to output a reduced image  
1b.

In conclusion, a method for an image reducing processing circuit  
according to the present invention includes the memory architecture  
of two First-In-First-Out (FIFO) units, and the method firstly  
15 processes the horizontal direction image data and then processes the  
vertical direction image data, such that the memory depth of the  
first step First-In-First-Out (FIFO) unit is designed and is only  
substantially equal to that of the reduced image 1b. As the memory  
depth of the line buffers is equal to that of the original image 1a, the  
20 memory depth of the first step First-In-First-Out (FIFO) unit is less  
than that of the line buffers ( $1b < 1a$ ). By using the memory  
architecture of two First-In-First-Out (FIFO) units, the access  
frequency of the input processing unit, the horizontal direction  
image processing unit, the first step First-In-First-Out (FIFO) unit  
25 and the vertical direction image processing unit are simplified to the



first access frequency 1c only. The memory architecture of the second step First-In-First-Out (FIFO) unit is simplified to a one-input-one-output memory architecture, which only implements a transferring of the first and second access frequency 1c and 1d, so  
5 the memory depth of the second step First-In-First-Out (FIFO) unit  
24 is much less than that the original image 1a and the reduced image 1b.